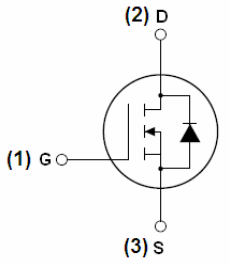
Description

The G3N50 is power MOSFET using advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

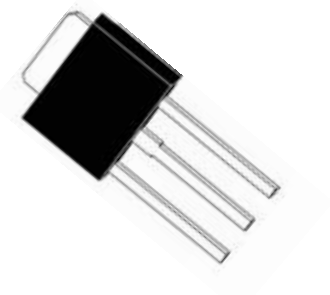


Schematic diagram

General Features

VDSS	RDS(ON) @10V (typ)	ID
500V	2.4Ω	3A

- Fast Switching (Rdson≤3.0Ω)
- Low ON Resistance
- Low Gate Charge (Typical Data8.5nC)
- Low Reverse transfer capacitances(Typical :4.5pF)
- 100%Single Pulse avalanche energy Test



TO-251

Application

- Power switch circuit of electron ballast and adaptor

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±30	V
Drain Current-Continuous	I_D, T_C=25℃	3	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	2.3	A
Pulsed Drain Current	I_{DM}	12	A
Maximum Power Dissipation	P_D	35	W
MOSFET dv/dt RUGGEDNESS	dv/dt	5	V/ns
Single pulse avalanche energy (Note 5)	$_JE_{AS}$	64	mJ
Operating Junction and Storage Temperature Range	T ,T_{STG}	150,-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	0.28	℃ /W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	500	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=500V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0		4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=1.5A	-	2.4	3.0	Ω
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	280	-	PF
Output Capacitance	C_{oss}		-	37	-	PF
Reverse Transfer Capacitance	C_{rss}		-	4.5	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{GS}=10V,I_D=3A, V_{DS}=250V,R_{GEN}=18Ω	-	8	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	31	-	nS
Turn-Off Fall Time	t_f		-	17	-	nS
Total Gate Charge	Q_g	V_{DS}=250 V,I_D=3A, V_{GS}=10V	-	8.5	-	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	nC
Gate-Drain Charge	Q_{gd}		-	3.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_{SD}=5A	-	-	1.5	V
Diode Forward Current (Note 2)	I_S		-	-	3	A
Reverse Recovery Time	t_{rr}	V_{DD}=100V, I_{SD}=3A di/dt = 100A/μs(Note3)	-	135		nS
Reverse Recovery Charge	Qrr		-	400		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: Tj=25℃,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω

Characteristics Curve:

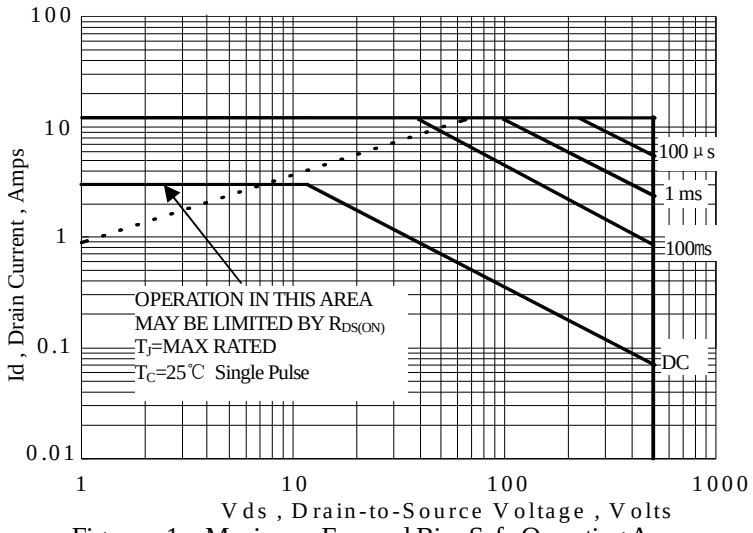


Figure 1 Maximum Forward Bias Safe Operating Area

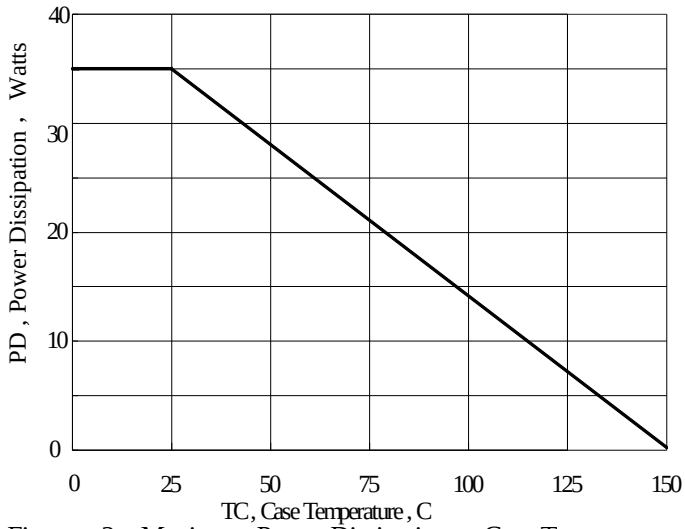


Figure 2 Maximum Power Dissipation vs Case Temperature

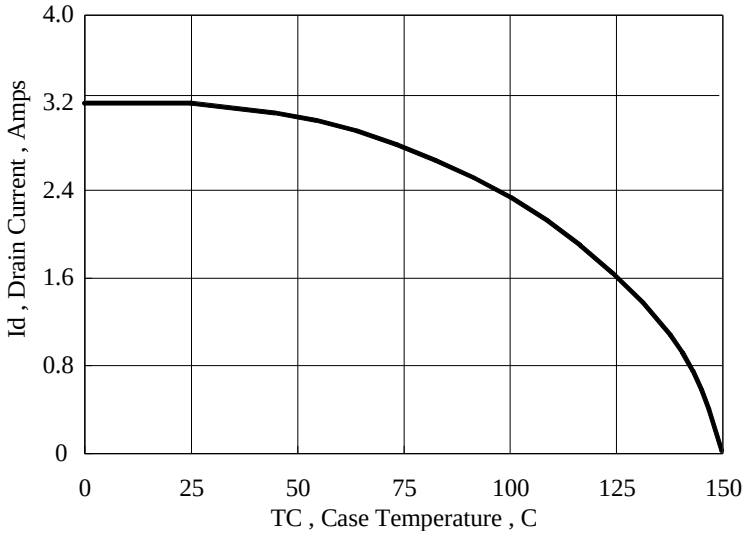


Figure 3 Maximum Continuous Drain Current vs Case Temperature

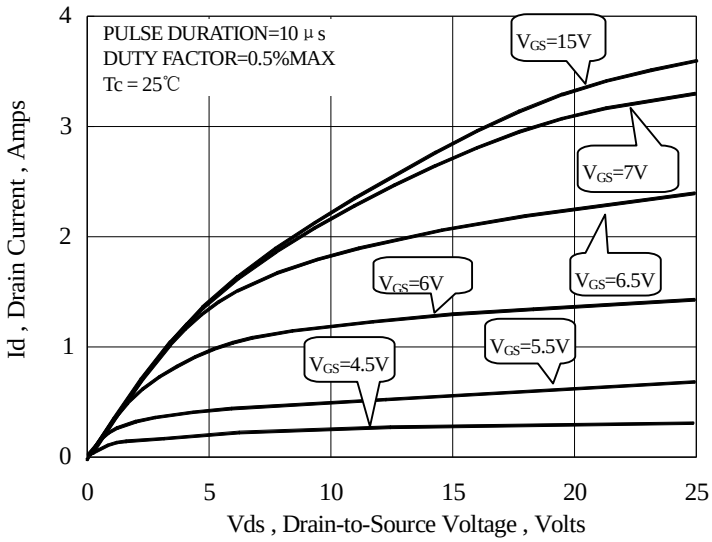


Figure 4 Typical Output Characteristics

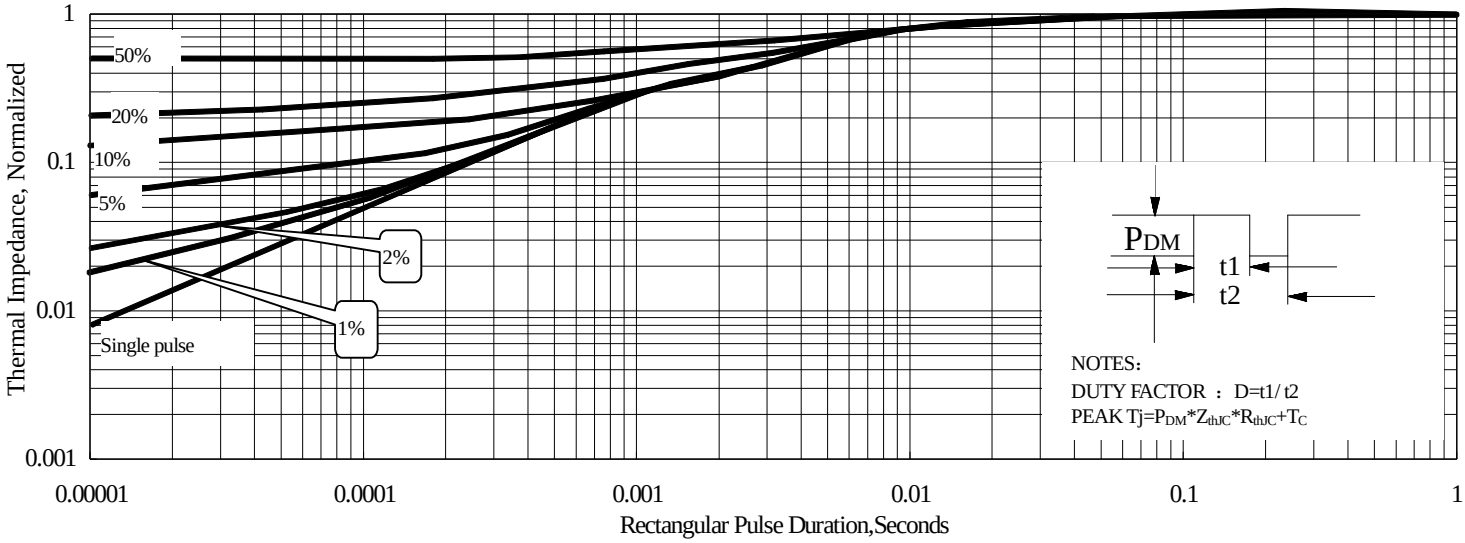


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

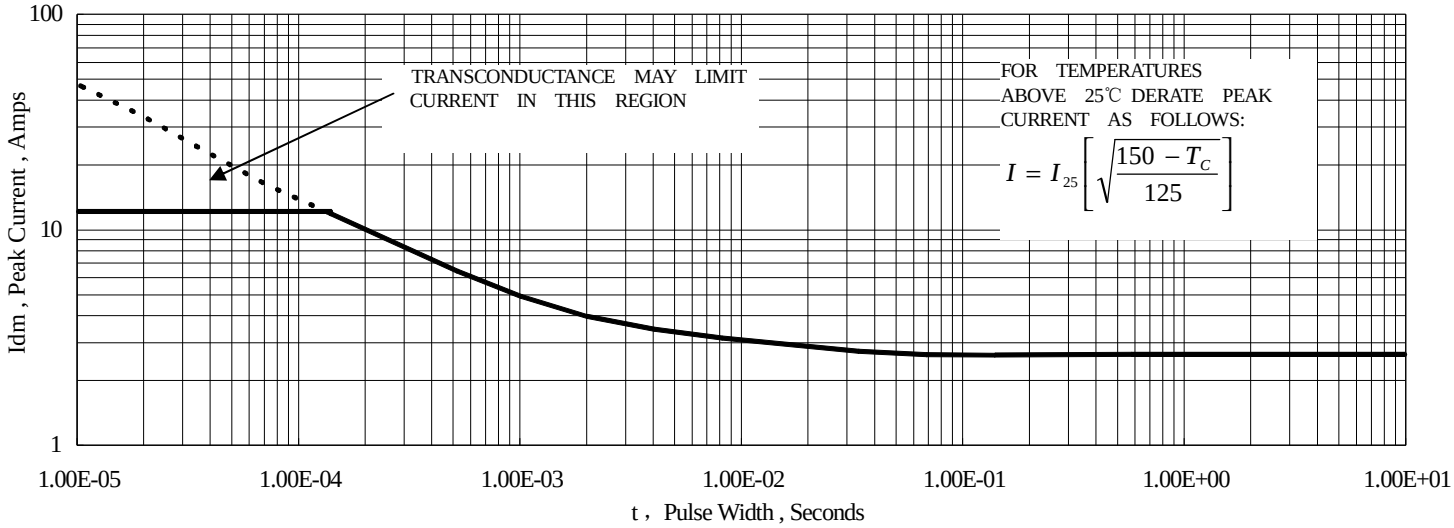


Figure 6 Maximum Peak Current Capability

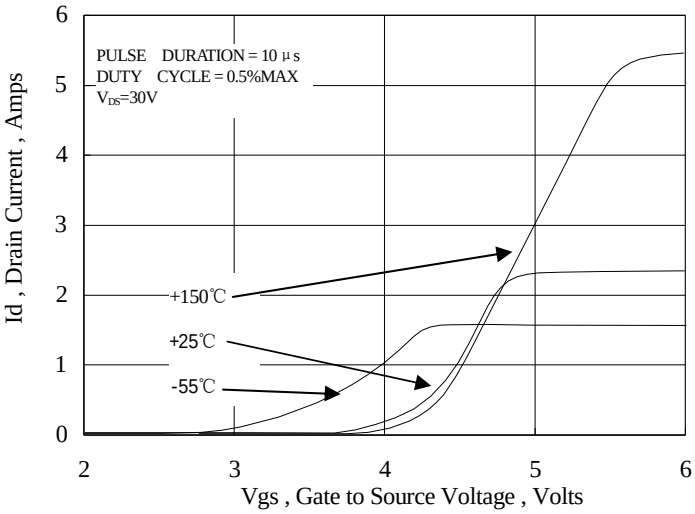


Figure 7 Typical Transfer Characteristics

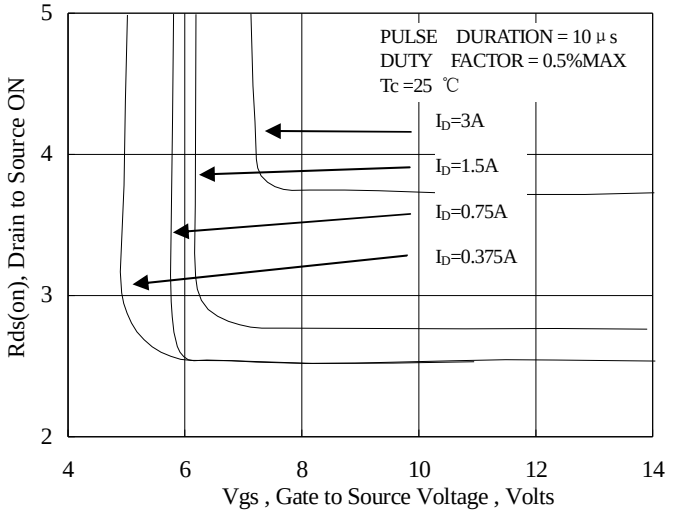


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

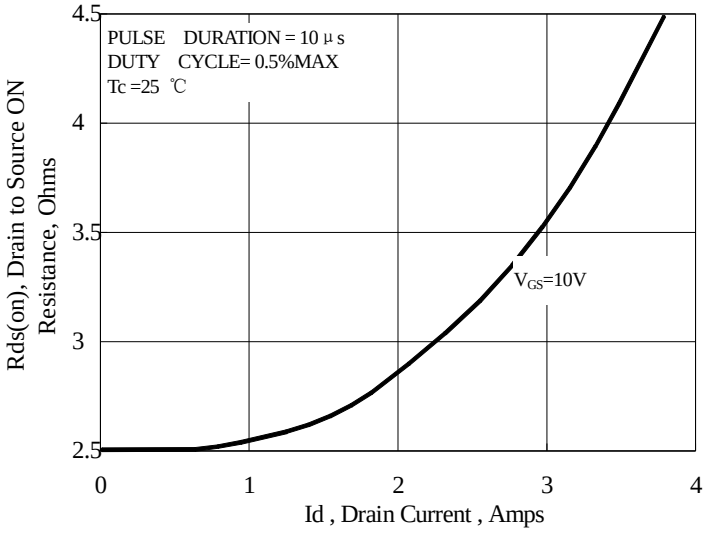


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

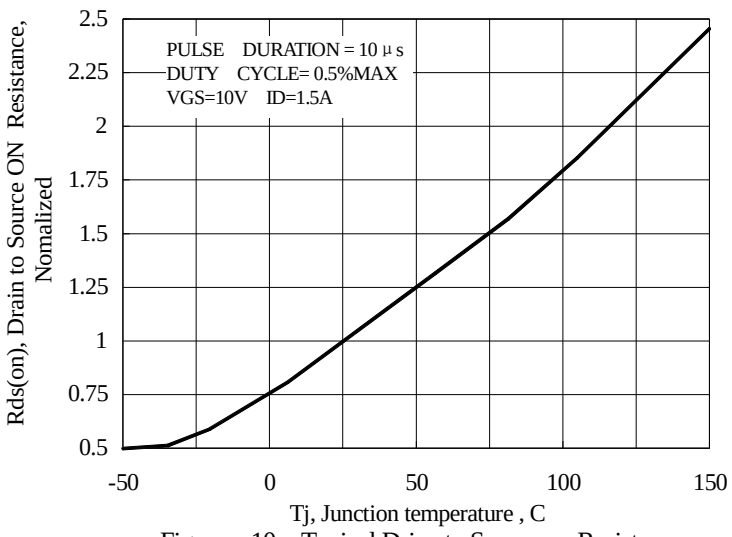


Figure 10 Typical Drian to Source on Resistance vs Junction Temperature

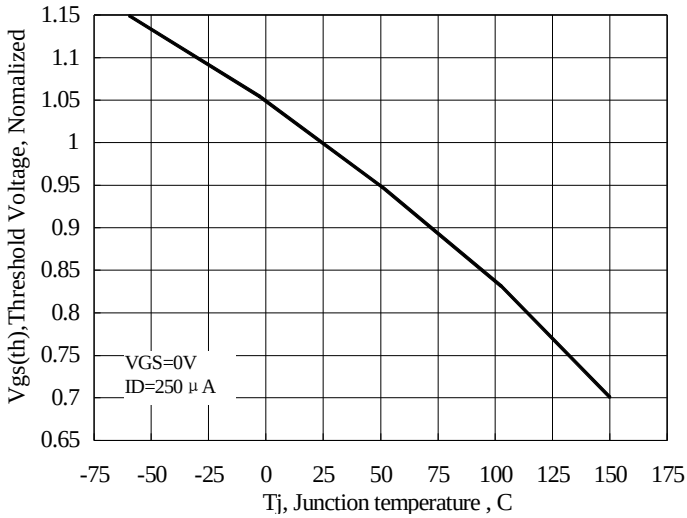


Figure 11 Typical Theshold Voltage vs Junction Temperature

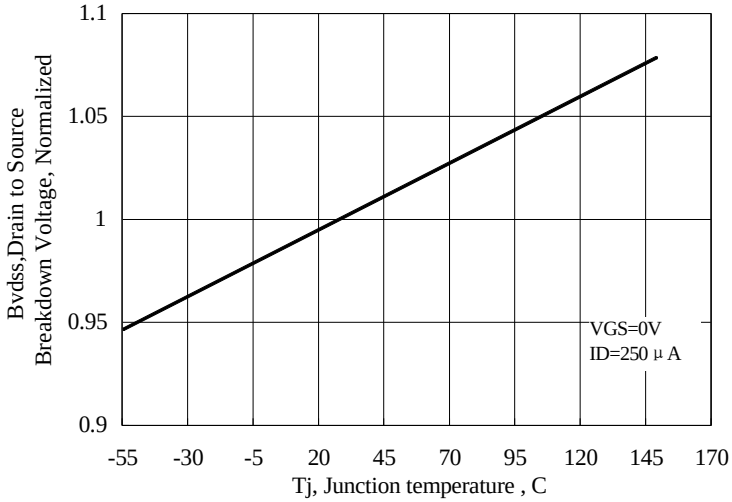


Figure 12 Typical Breakdown Voltage vs Junction Temperature

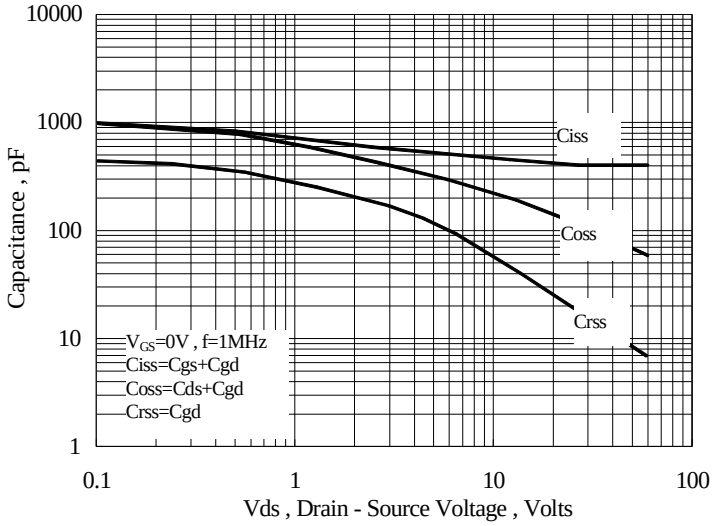


Figure 13 Typical Capacitance vs Drain to Source Voltage

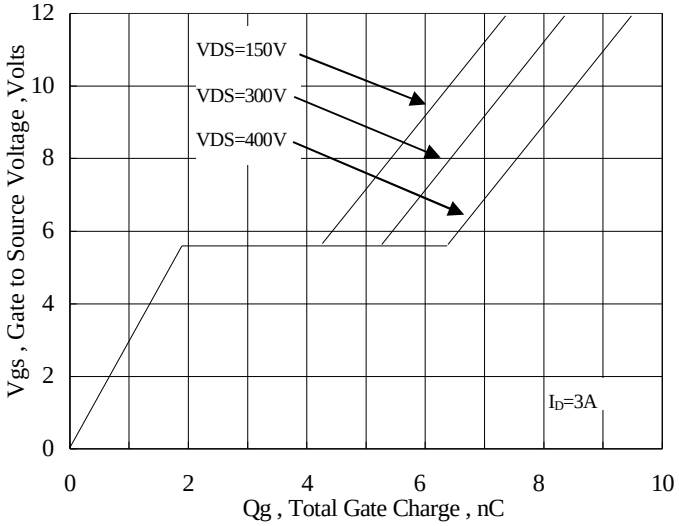


Figure 14 Typical Gate Charge vs Gate to Source Voltage

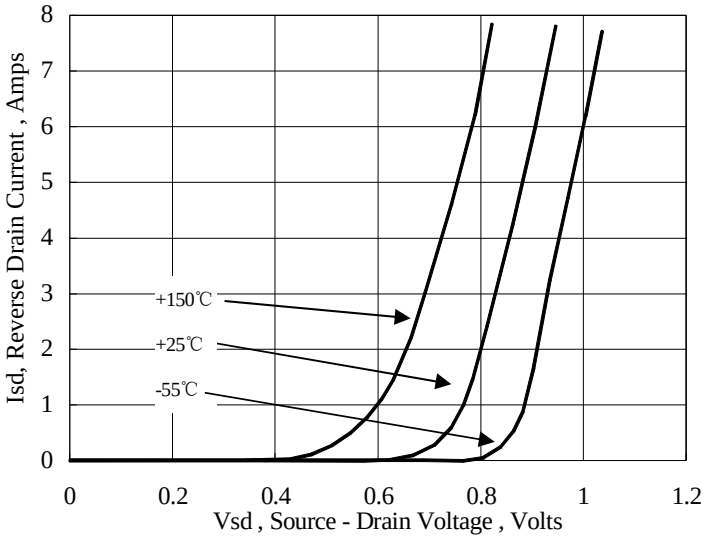


Figure 15 Typical Body Diode Transfer Characteristics

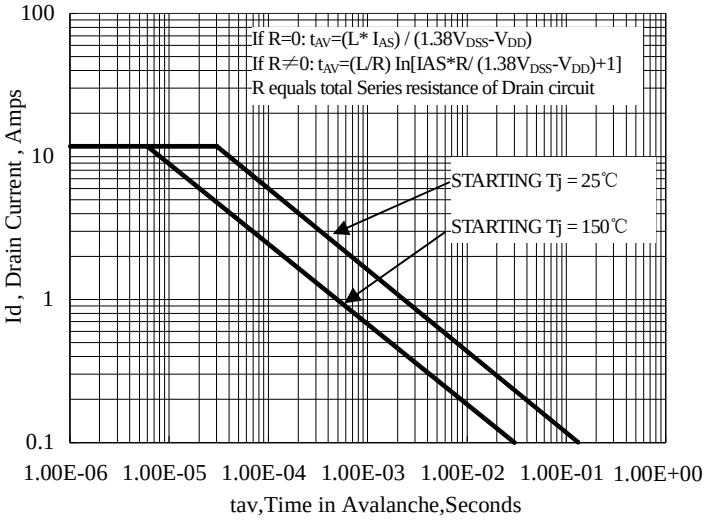


Figure 16 Unclamped Inductive Switching Capability

Test Circuit and Waveform

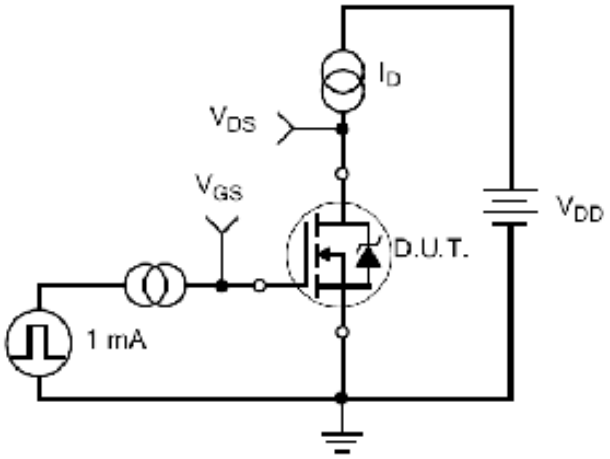


Figure 17. Gate Charge Test Circuit

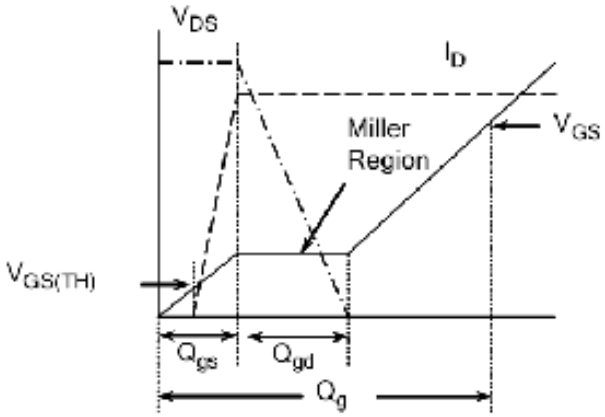


Figure 18. Gate Charge Waveform

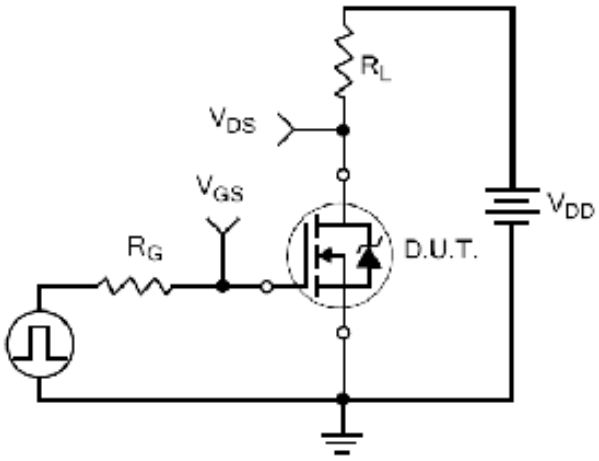


Figure 19. Resistive Switching Test Circuit

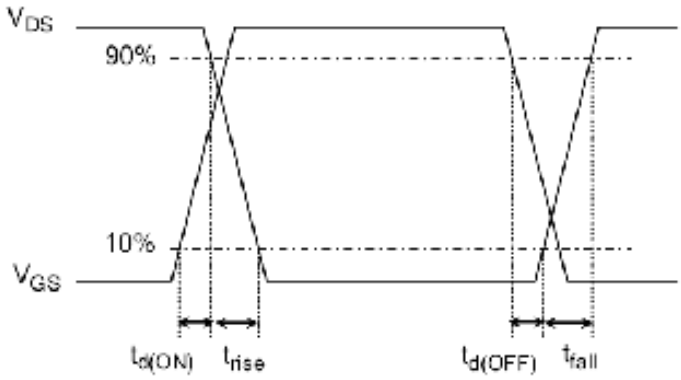


Figure 20. Resistive Switching Waveforms

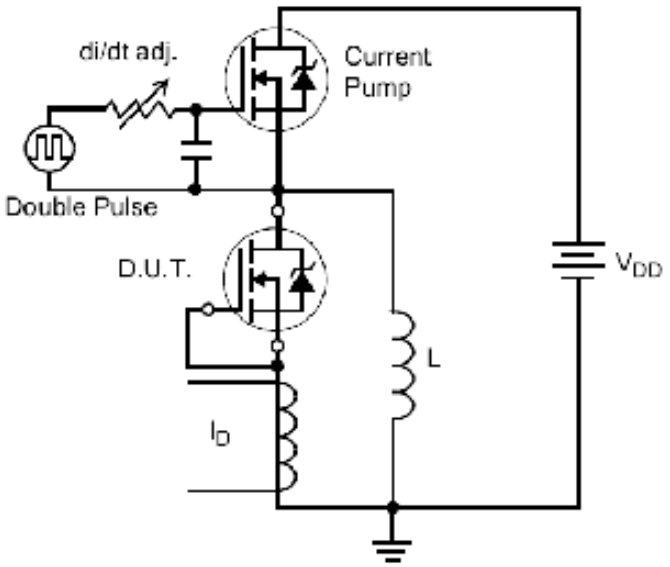


Figure 21. Diode Reverse Recovery Test Circuit

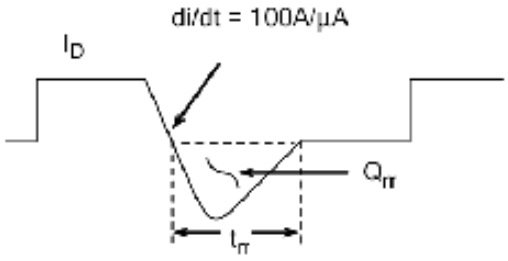


Figure 22. Diode Reverse Recovery Waveform

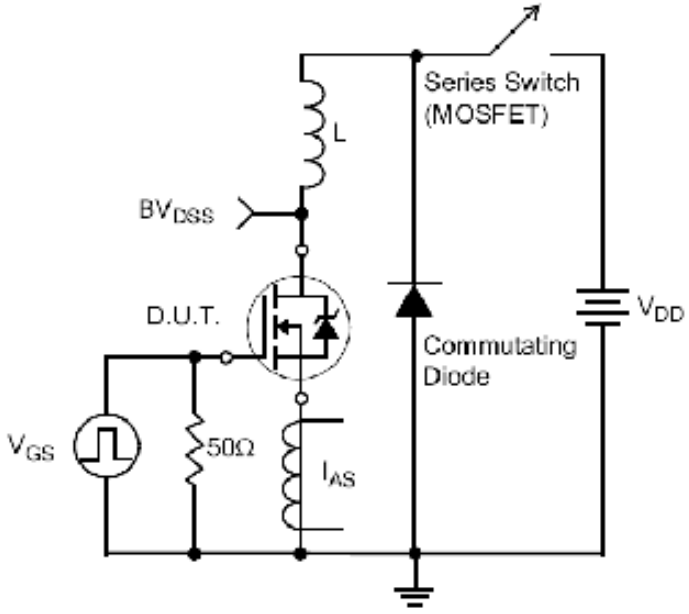


Figure 23. Unclamped Inductive Switching Test Circuit

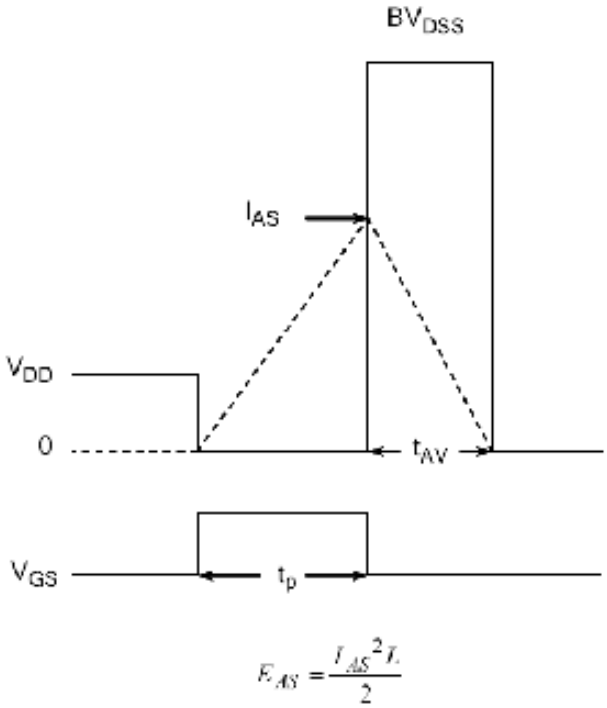


Figure 24. Unclamped Inductive Switching Waveforms